REMARKS

Claims 1-21 remain pending in the application.

In the Office Action, the Examiner objected to the specification; rejected claims 1-8 under 35 U.S.C. § 102(b) as being anticipated by Jones et al. (U.S. Patent No. 6,078,595); and rejected claims 9-21 under 35 U.S.C. § 103(a) as being unpatentable over Jones et al. in view of Richardson et al. (U.S. Patent No. 6,356,532).

The objection to the specification has been obviated by the above amendment to paragraph 0002.

Claims 1-8:

Applicant respectfully traverses the § 102(b) rejection of claims 1-8 over Jones et al. Independent claim 1 recites a panel including, *inter alia*, "a first side, including: at least one first connector . . . and a plurality of second connectors . . . ; and a second side opposite from the first side, including: a plurality of third connectors . . ." Jones et al. fails to teach all elements of the panel of claim 1.

Page 2 of the Office Action reads the claimed "at least one first connector" on elements 12a and 12b in Fig. 1 of Jones et al. Page 2 also reads the claimed "plurality of second connectors" on the PORT 4s in Fig. 7 of Jones et al. Finally, page 2 reads the claimed "plurality of third connectors" on element 44 in Fig. 5 of Jones et al. The cited portions of Jones et al. fail to anticipate claim 1 for at least the following reasons.

Of the three elements cited in the Office Action, two are not "connectors" at all. Jones et al. discloses that elements 12a and 12b are "timing modules (TMs)" (col. 4, line 12) and that these TMs 12a/b include circuitry such as a stratum 3 (STR 3) clock module 16, an internal clock

24, and a phase-locked loop (PLL) 26 (Fig. 1; and col. 4, lines 35-49). Timing modules including various timing circuitry do not correspond to the plain meaning of "at least one first connector," so TMs 12a/b in Jones et al. do not teach this claimed feature. Similarly, Jones et al. discloses that element 44 in Fig. 5 is a "line interface unit (LIU)" that "provides a digitized version of the external reference" and that "provides various error checking functions" (col. 6, lines 2, 3, and 8). Line interface units that provide digitizing and error checking do not correspond to the plain meaning of "a plurality of third connectors," so LIUs 44 in Jones et al. do not teach this additional claimed feature.

Even if interfaces associated with these elements of Jones et al. could be properly[1] read on the first through third connectors in claim 1, the TMs 12a/b, PORT 4s, and LIUs 44 disclosed by Jones et al. do not meet the structural requirements of claim 1. Independent claim 1 recites that the first connector, the plurality of second connectors, and the plurality of third connectors are all included in "a panel." By contrast, Jones et al. discloses that TMs 12a/b (which include LIUs 44 as shown in Fig. 5) are *physically separated* from physical layer (PHY) cards 22 (which include PORT 4s as shown in Fig. 7) by a Base I/O (BIO) card 20 and a backplane (see Fig. 1 and col. 2, lines 51-55). Thus, Jones et al. fails to teach all features of claim 1, at least because TMs 12a/b, PORT 4s, and LIUs 44 are not included in "a panel" as set forth in the claim.

Further, claim 1 recites that a first side of the panel includes the at least one first connector and the plurality of second connectors. Because TMs 12a/b (which are alleged to correspond to the claimed first connector) and the PORT 4s (which are alleged to correspond to the claimed plurality of second connectors) on PHY cards 22 are physically separated, Jones et

[1] Not every electrical connection in a circuit or system corresponds to a "connector."

al. fails to teach a first side of the panel that includes both "at least one first connector" and "a plurality of second connectors," as set forth in claim 1.

Claim 1 also recites that a second side opposite from the first side includes a plurality of third connectors. By contrast, Fig. 5 of Jones et al. discloses that LIUs 44 (which are alleged to correspond to the claimed plurality of third connectors) are included in TMs 12a/b (which are alleged to correspond to the claimed first connector). Because, LIUs 44 are included in TMs 12a/b, and not on an opposite side of a panel from TMs 12a/b, Jones et al. fails to teach a plurality of third connectors on a "second side [of a panel] opposite from the first side" that includes at least one first connector, as set forth in claim 1.

Because Jones et al. fails to teach all elements of independent claim 1 arranged as required by the claim, the § 102(b) rejection of the claim is improper, and should be withdrawn. Dependent claims 2-8 are allowable at least by virtue of their dependence from claim 1.

Claims 9-21:

Applicant respectfully traverses the § 103(a) rejection of claims 9-21 over Jones et al. in view of Richardson et al. Assuming, purely for the sake of argument, the propriety of adding teachings from Richardson et al., such addition fails to cure the deficiencies of Jones et al. explained extensively above with regard to claims 1-8. Page 4, paragraph 13, of the Office Action implies that Richardson et al. is cited solely for its teaching of jacks for testing via a patch cable. The combination of Jones et al. and Richardson et al. fails to teach or suggest all elements of claims of 9-21, and a *prima facie* case of obviousness has not been established for these claims, for the following reasons.

Independent claim 9 recites a timing output panel including, *inter alia*, "a rear portion,

including: a plurality of network connectors . . . and at least one timing connector . . . ; and a front portion, including: a plurality of equipment jacks . . . and a plurality of timing jacks . . ." Page 3 of the Office Action alleges that PORT 4 of PHY card 22 in Jones et al. corresponds to the claimed "plurality of network connectors" and page 4 alleges that TMs 12a/b of Jones et al. correspond to the claimed "at least one timing connector."

As explained above with regard to claim 1, TMs 12a/b are timing modules that contain timing circuits and do not reasonably teach or suggest a "timing connector." Further, Jones et al. fails to teach or suggest a timing output panel including both a front portion and a rear portion, as set forth in claim 9. Also, TMs 12a/b and PORT 4s on PHY cards 22 are physically separated, so Jones et al. fails to teach or suggest a "rear portion" of an output panel that includes both "at least one timing connector" and "a plurality of network connectors," as recited in claim 9. Richardson et al. is not alleged to, and does not, cure these deficiencies of Jones et al. Thus, a *prima facie* case of obviousness has not been made for claim 9, at least because the references when combined fail to teach or suggest all elements of the claim. Claims 10-16 are allowable at least by virtue of their dependence on claim 9.

Independent claim 17 recites a panel including, *inter alia*, "a rear portion, including: means for connecting to a plurality of network elements, and means for connecting to synchronization electronics; and a front portion, including: means for testing . . ." As explained above with regard to claim 1, Jones et al. fails to teach or suggest at least a panel including both a front portion and a rear portion, as set forth in claim 17. Richardson et al. is not alleged to, and does not, cure this deficiency of Jones et al. Thus, a *prima facie* case of obviousness has not been made for independent claim 17, at least because the references when combined fail to teach

or suggest all elements of the claim.

Further, the Office Action does not read the elements of claim 17 on either of the applied references. Nowhere on pages 3-5 does the Office Action read the "means for connecting to a plurality of network elements," the "means for connecting to synchronization electronics," or the "means for testing . . ." on any portion of Jones et al. or Richardson et al. M.P.E.P. § 2142 states that "[t]he Examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness." The Office Action does not mention the above-quoted elements of claim 17, so the conclusion of obviousness has not been factually supported for this claim. A *prima facie* case of obviousness has not been made for independent claim 17 for at least this additional reason. Claims 18-20 are allowable at least by virtue of their dependence on claim 17.

Independent claim 21 recites a system including, *inter alia*, "a plurality of network elements . . . ; a timing signal generator . . . ; and a timing output panel connected between the plurality of network elements and the timing signal generator, the timing output panel including: at least one first connector . . . , a plurality of second connectors . . . , and a plurality of third connectors spaced apart from the first and second connectors . . ." Nowhere on pages 3-5 does the Office Action read the "plurality of network elements," or the "timing signal generator" on any portion of Jones et al. or Richardson et al. As explained above with regard to claim 17, the failure to mention these elements of claim 21 does not factually support the conclusion of obviousness for this claim. For at least this reason, a *prima facie* case of obviousness has not been established for independent claim 21.

Further, to the extent that page 4, line 1, of the Office Action reads the TMs 12a/b in Jones et al. on one of the connectors in claim 21, Applicant again notes that timing modules that

contain timing circuits do not reasonably teach or suggest a "connector." A *prima facie* case of obviousness also has not been established for independent claim 21, at least because the references when combined fail to teach or suggest all elements of the claim.

Claims 1-21 are allowable over the applied art. Reconsideration of the rejections and allowance of these claims are respectfully requested.

In the event that any outstanding matters remain in this application, Applicant requests that the Examiner contact the undersigned at the number below to discuss such matters.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 13-2491 and please credit any excess fees to such deposit account.

Respectfully submitted,

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